REMARKS

Prior to a first examination, please enter the foregoing amendments and the following remarks. A first examination of this case is respectfully requested in view of the foregoing amendments and the following remarks.

Claims 1-13 and 19-20 have been cancelled without prejudice. Claims 21-29 have been added by this preliminary amendment. Claim 15 has been amended herein. Accordingly, claims 14-18 and 21-29 remain at issue in the application. Of the pending claims, claims 14, 22, and 28 are independent claims.

Applicant believes that no new matter has been added through this preliminary amendment.

I. Divisional Application

The application papers filed herewith are a true copy of the prior complete application filed on September 8, 2002 by inventors Kumar Ganapathy and Ruban Kanapathippillai having US Patent Application Serial No. 10/215,721 and also filed on January 31, 2000 by inventors Kumar Ganapathy and Ruban Kanapathippillai having US Patent Application Serial No. 09/494,608.

The divisional application filed herewith under Rule 1.53(b) claims the benefit of the US Patent Application Serial No. 10/215,721 and its filing date of September 8, 2002 under 35 U.S.C. 120 and 37 CFR 1.78(a), which is a divisional and claims the benefit of the US Patent Application Serial No. 09/494,608 and the filing date of January 31, 2000.

II. Restriction Requirement/Claims

Claims 1-20 of the parent patent application Serial No. 09/494,608 were restricted into multiple groups.

Claims 14-18 of the parent patent application 09/494,608 were restricted to Group III as being drawn to an instruction set architecture (ISA) for executing dyadic instruction for calculating the specific type of D=(A op1 B) op2 C, classified in class 712, subclass 221 and subsequently restricted in US Patent Application Serial No. 10/215,721.

Claims 1-13 and 19-20 originally within the parent patent application, US Patent Application Serial No. 09/494,608, have been or are currently being prosecuted in other patent applications and are canceled herein without prejudice.

Claims 14-18 of the parent patent application Serial No. 09/494,608 are now pending for examination.

In the Office Action mailed on 02/11/23003 in Application No. 10/215,721, a first restriction requirement restricted claims numbering 14-18 and 21 to Group I as being "drawn to an Instruction Set Architecture with including instructions to perform (A op1 B) op2 C function, classified in class 712, subclass 200." In response to the first restriction requirement, Applicant elected to prosecute Group II claims. Applicant now presents these Group I claims 14-18 and 21 for a first examination on the merits.

In the Office Action mailed on 07/16/23003 in Application No. 10/215,721, a second restriction requirement restricted claims numbering 31-37 and 44 to Group II as being "drawn to an Instruction Set Architecture with control instructions for RISC control unit to control execution of DSP instructions in a plurality of DSP units, classified in class 712, subclass 200." In response to the second restriction requirement, Applicant elected to prosecute Group I claims. For a first examination on

the merits, Applicant now represents these Group II claims as new claim numbers 22-26, 27, and 28-29 corresponding to the restricted claims 31-35, 44, and 36-37, respectively.

III. Title

Applicant respectfully requests that the Title of the Application be changed to:

"INSTRUCTION SET ARCHITECTURE FOR SIGNAL PROCESSORS"

IV. Specification

Applicant has added a Cross-Reference to Related Applications section, on page 2, line 6, to reflect the cross-noted applications to which this divisional patent application claims the benefit thereof.

V. Claim Amendments

Claim 15 has been amended by this preliminary amendment.

The parenthetical "(i.e. mode registers)" was deleted from claim 15 for clarification. The phrase "mode registers" in claim 15 was amended to --mode bits-- to correspond with the clarification.

Applicant believes this amendment to claim 15 clarifies the claim and was not made for reasons of patentability.

CONCLUSION

A first examination of the pending claims is respectfully requested. Allowance of the claims at an early date is hereby respectfully solicited.

The Examiner is invited to contact Applicant's undersigned counsel by telephone at (714) 557-3800 to expedite the prosecution of this case should there be any unresolved matters remaining.

Please charge any shortage in fees in connection with the filing of this paper to Deposit Account 02-2666 and please credit any excess fees to such deposit account.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Dated: September 19, 2003

William E. Alford
Reg. No. 37,764

IN THE TITLE

Please amend the Title of the Application as follows:

"~~METHOD AND APPARATUS FOR~~ INSTRUCTION SET ARCHITECTURE FOR SIGNAL PROCESSORS ~~HAVING DYADIC DIGITAL SIGNAL PROCESSING INSTRUCTIONS~~".